DSP Implementation of A Stereo Echo Canceller with A Single Adaptive Filter per Channel

1チャンネル1個の適応フィルタで構成される多チャンネルエコーキャンセラのハードウエア実現

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ABSTRACT

This paper presents an implementation of a stereo echo canceller by digital signal processors (DSPs). In this implementation, flexibility and extensibility is considered for evaluation and improvement of the echo cancellation algorithm. A newly-developed multiple-DSP system with NEC's μPD77230 32-bit floating point DSPs has extensible construction and flexible inter-DSP communication channels. More complex system can be realized by increasing the number of the DSP boards. Twelve DSPs are used for realizing the stereo echo canceller. The experimental results show that this echo canceller can achieve sufficient echo return loss enhancement for a white noise. Satisfactory subjective quality is also provided for real speech signals.

1. INTRODUCTION

Acoustic echo cancellers are necessary for communication systems such as TV conference systems and hands-free telephones. A large number of taps required for these applications makes the echo cancellers difficult to be implemented. This problem is more serious for a conventional multi-channel echo canceller based on linear combination[1]. A new multi-channel echo canceller, which needs a single adaptive filter per channel, has been proposed. It requires approximately half the number of total taps of the linear combination in a stereo case. Thus, it makes implementation easier. Even for this compact multi-channel echo canceller, there are still some obstacles to be overcome.

Digital signal processors (DSPs) are widely used to realize acoustic echo canceller for experiments. However, necessary amount of computations is far more than what is possible by a single DSP. Multiple DSP solution is essential for this application. It can also provide flexible and extensible system.

The purpose of this paper is to show the feasibility using multiple DSPs and the performance of the compact stereo echo canceller. Section 2 briefly reviews the algorithm of the implemented stereo echo canceller. The configuration of a multi-channel digital signal processing system developed for this implementation is shown in Section 3, followed by the implementation of the echo canceller. Finally, experimental results are demonstrated to show the performance.

2. A STEREO ECHO CANCELLER WITH A SINGLE ADAPTIVE FILTER PER CHANNEL

As a multi-channel echo canceller, it is natural to use adaptive filters which have one-to-one correspondence to the echo paths. A multi-channel echo canceller based on linear combination[1] is derived from this idea. This echo canceller has two problems; hardware size and convergence. In a stereo case, its hardware size is four times larger than a monaural case while the number of channel is only twice larger. The filter coefficients do not converge to their optimum values for cross correlated input signals[3]. Such problems are overcome by a compact multi-channel echo canceller with a single adaptive filter per channel[2].

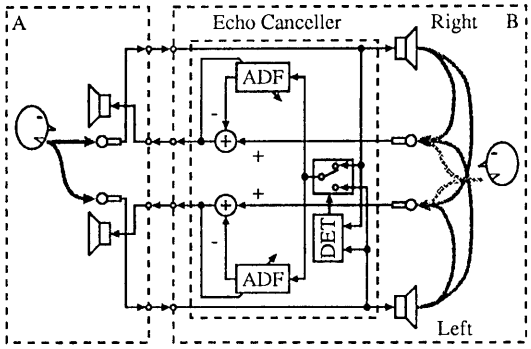


Fig. 1. Block diagram of a stereo echo canceller with a single adaptive filter per channel.

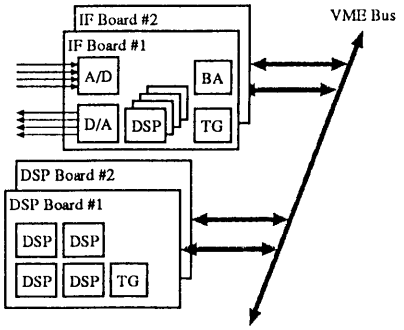


Fig. 2. Block diagram of a multi-channel digital signal processing system.

The block diagram of the compact stereo echo canceller is shown in Fig. 1. This echo canceller has two adaptive filters, one for the right channel and the other for the left channel. Each adaptive filter generates an echo replica for the corresponding channel. Both adaptive filters use the same input signal which is ahead in phase between the two as their input signals. This condition on the input signal selection is imposed in order to satisfy the law of causality between the adaptive filter input and the echo. The detector (DET) is used for detecting such an input signal. It is accomplished by examining the polarity of the time difference between the signals which maximizes the cross-correlation.

In order to implement the stereo echo canceller, an approach using DSPs is selected because of its flexibility. A general purpose multi-channel digital signal processing system has been developed and is used for this implementation.

3. Multi-Channel Digital Signal Processing System

A multi-channel digital signal processing system provides multiple analog-to-digital (A/D) converters, digital-to-analog (D/A) converters and DSPs. This system consists of interface (IF) boards and DSP boards as shown in Fig. 2. The IF board is capable of four-channel A/D and D/A (analog-digital) conversion. The number of channel can be increased by simply using additional IF boards. Increase

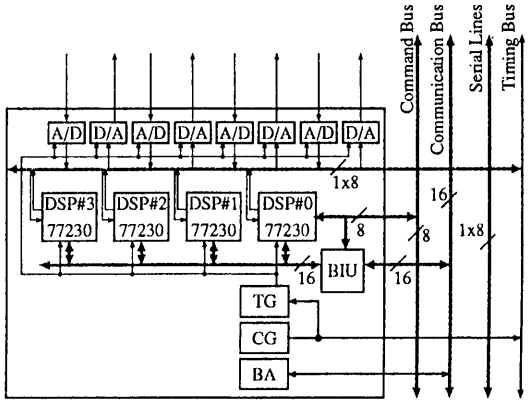


Fig. 3. Block diagram of the IF board.

of the number of DSP boards makes more complex system with more computations possible.

Both the IF board and the DSP board can be equipped with up to four NEC's μPD77230 32-bit floating point DSPs[4]. All the DSPs work in the slave mode. The DSP has a pair of serial input-output (I/O) ports, an 8-bit data bus and a 16-bit host interface bus. The data bus is used to access external RAMs and I/O registers. The host interface bus is used for inter-DSP communication.

3.1. IF Board

The IF board consists of four A/D converters, four D/A converters, up to four DSPs, a clock generator (CG), a timing generator (TG), a bus interface unit (BIU) and a bus arbiter (BA) as shown in Fig. 3. A one-chip

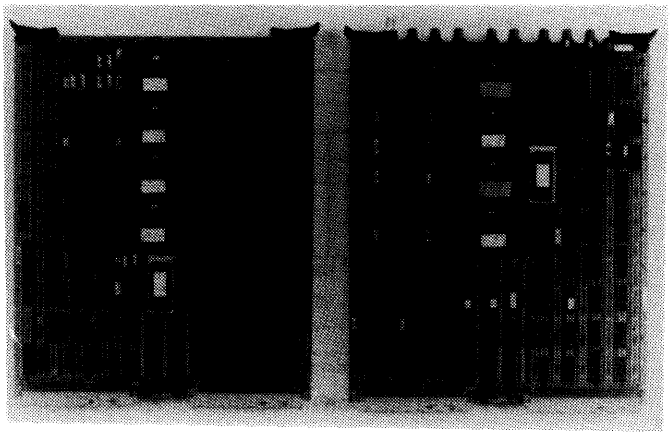


Fig. 4. IF board(right) and DSP board(left).

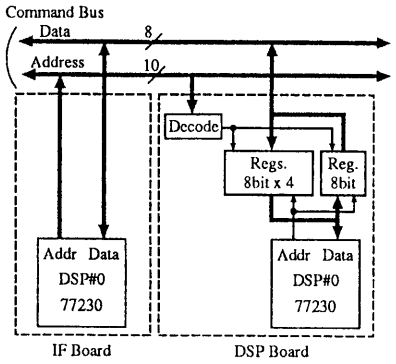


Fig. 6. Command bus.

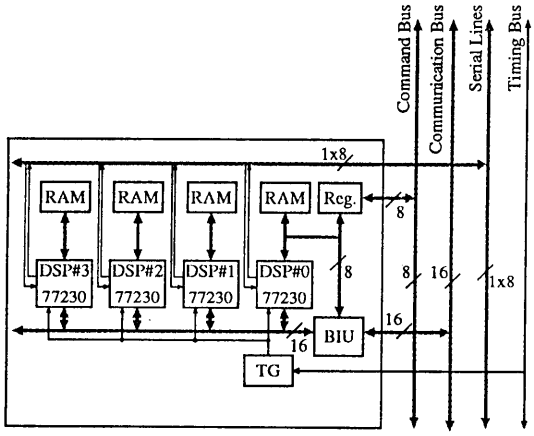


Fig. 5. Block diagram of the DSP board.

μ-law CODEC μPD9602AD, which consists of an A/D converter, a D/A converter and two anti-aliasing filters, is used for analog-digital conversion. The sampling rate is 8KHz.

The serial data clock and the DSP clock are generated by the CG. The serial I/O timing signals for μ-law CODECs and DSPs are derived from the TG. It also generates the reset and the interrupt signals for DSPs. The BIU and the BA are used for inter-board communication. Fig. 4 shows the developed IF board and the DSP board.

3.2. DSP Board

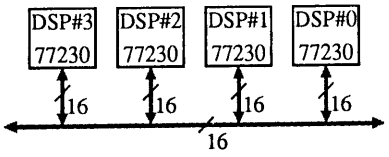
The DSP board is equipped with up to four DSPs with a 32KB external RAM for each DSP, a TG and a BIU. The serial data clock and DSP clock are supplied from the IF board. The TG provides DSPs with the serial I/O timing signals, the reset signals and the interrupt signals. The BIU is used for inter-board communication.

3.3. Communication Channels

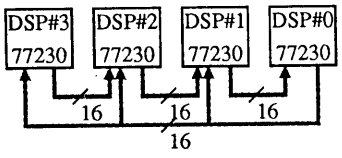
Four types of communication channels, i.e. eight serial lines, an 8-bit command bus, 16-bit intra-board communication buses and a 16-bit inter-board communication bus, are used for data transmission between DSPs and μ-law CODECs. Eight independent serial lines can be used for both intra-board and inter-board communication. The μ-law CODECs are connected to DSPs by the serial lines. Bit rate is 2M bit/sec. The transmission timing is determined by TGs.

By using the command bus, the IF board can write commands and parameters into four 8-bit registers on the DSP board. The IF board can also read the status of a DSP board from an 8-bit register on the DSP board. The target DSP board is specified by the address bus. The configuration of the command bus is shown in Fig. 6.

The intra-board communication bus on both the IF board and the DSP board physically connects four DSPs as shown in Fig. 7 (a). Fig. 7 (b) show the logical connection of this bus. The DSP#0 can transmit data to all



(a) Physical Connection



(b) Logical Connection

Fig. 7. Intra-board communication bus.

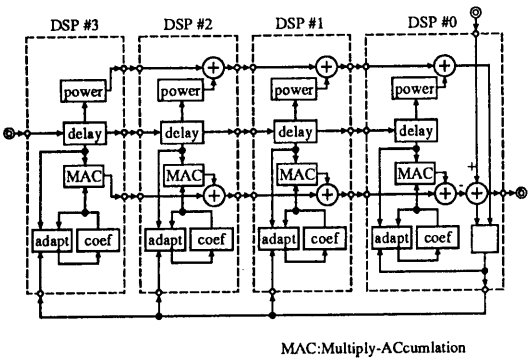


Fig. 8. Implementation of an FIR adaptive filter.

the other three DSPs simultaneously while the other three DSPs can transmit data only to their neighboring DSP in the right. This structure is suitable for realizing an adaptive filter by connecting DSPs. A filter can be realized by cascade connection of four sub-filters. Fig. 8 shows an FIR adaptive filter with Learning Identification Method (LIM)[5].

The inter-board communication bus supports data transmission between DSPs on different boards. It is shared by all IF boards and DSP boards as in Fig. 9. All the IF boards and the DSP boards act as either a bus master board or a bus slave board. One of the IF boards also acts as the BA. Up to eight boards can be used as the bus master boards. The maximum number of the bus slave board is 128. The communication sequence by using this bus is as follows:

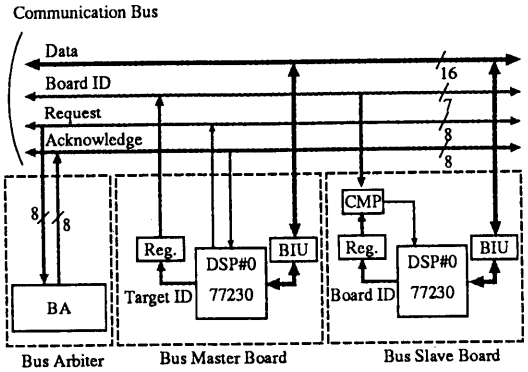


Fig. 9. Inter-board communication bus.

(1) A bus master board requests bus access permission.
(2) The BA gives bus access permission to one of the bus master boards which made requests.
(3) The permitted bus master board sends the target board ID, which specifies the destination board, to the board ID bus.
(4) The bus slave board corresponding to target board ID responds to the bus master board.
(5) Data transmission starts.

Flexible communication could be realized since the bus master board dynamically changes the target board.

4. IMPLEMENTATION OF A STEREO ECHO CANCELLER

The stereo echo canceller is implemented by using one IF board and two DSP boards as shown in Fig. 10. Each DSP board is used as an adaptive filter. A controller for the echo canceller, the detector and the selector are realized by the DSPs on the IF board. The control commands for the echo canceller, such as filter-coefficient initialization and echo-canceller activation, are generated in the IF board and transmitted to the DSP boards. Each DSP on the IF board receives either the echo or the input signal in μ-law format from the connected A/D converter and converts it to floating point data. A DSP on the IF board detects the input signal which is ahead in phase and sends the selected input signal to the

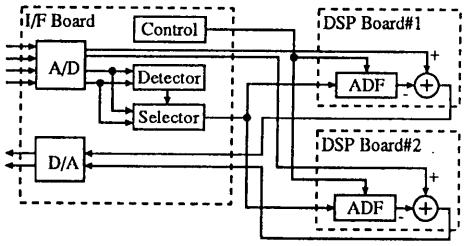


Fig. 10. Implementation of the stereo echo canceller.

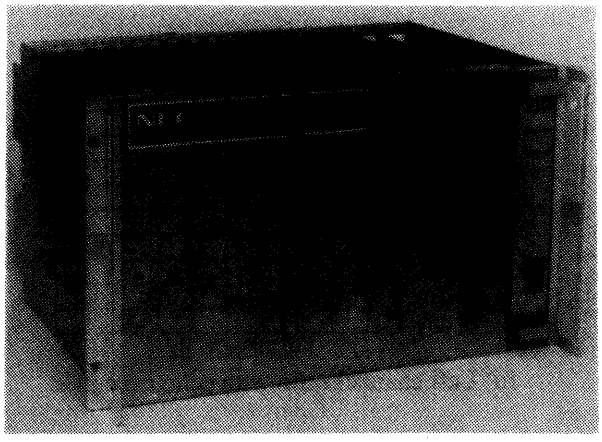


Fig. 11. Stereo echo canceller.

DSP boards. The echoes are also converted to floating point data and transmitted to the DSP boards.

A 512-tap FIR adaptive filter with LIM is realized by four DSPs on the DSP board as shown in Fig. 8. Each DSP is responsible for 128-tap convolution and filter-coefficient update. The residual echoes are converted to μ-law data and then sent to the D/A converters via the serial lines. Fig. 11 shows the developed stereo echo canceller. The specifications of the stereo echo canceller are shown in table 1.

5. EXPERIMENTAL RESULTS

Experiments for stereo echo cancellation have been performed for evaluation. The room size is about $10 \times 8 \times 3[m^3]$. The experimental set-up with the location of loudspeakers and microphones is shown in Fig. 12. The signal generator in an FFT analyzer generates a white

Table 1. Specifications of the stereo echo canceller.

Sampling rate	8[KHz]
Word length	8bit nonlinear(μ-law)
Number of taps	512

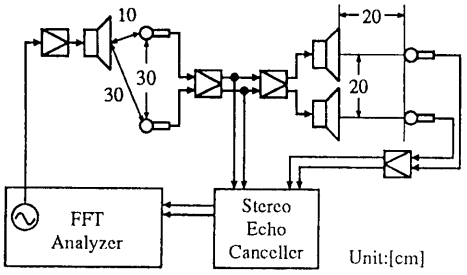


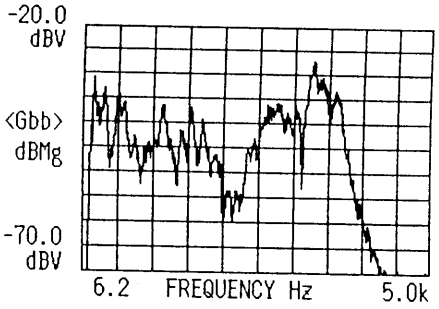
Fig. 12. Experimental set-up.

noise. Two microphones capture the propagated noise from the loudspeaker as far end signals. They are transmitted to the loudspeakers and the stereo echo canceller. The acoustic echoes are received by two microphones and are canceled by the echo canceller. The residual echoes are measured by the FFT analyzer.

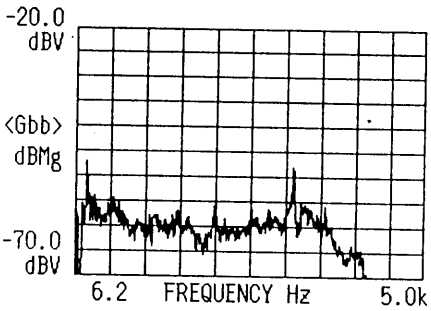
Fig. 13 shows experimental results. The mean echo return loss enhancement (ERLE) is about 15 [dB]. The reason of the low ERLE is the insufficient number of taps for such a large room. The results of subjective tests show that this echo canceller also can reduce echoes for real speech signals.

6. CONCLUSION

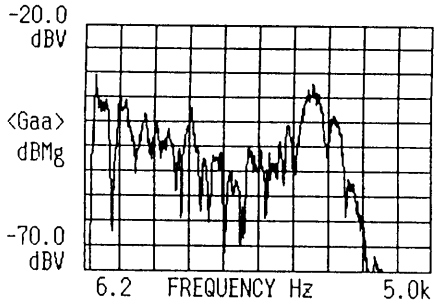
A stereo echo canceller with a single adaptive filter per channel has been implemented by using DSPs. A multi-channel digital signal processing system, which consists of IF boards and DSP boards, has been developed for this implementation. Two DSP boards for two 512-tap FIR adaptive filters and one IF board for analog-digital conversion are used for realizing the stereo echo canceller. Experimental results show that the implemented stereo echo canceller can reduce echoes for both white noises and real speech signals. The room used for the evaluation requires more



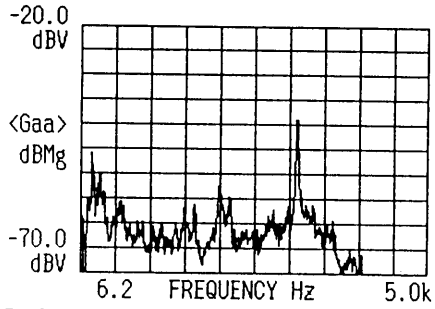
(a) Right channel echo without echo canceller.



(b) Right channel echo with echo canceller.



(c) Left channel echo without echo canceller.



(d) Left channel echo with echo canceller.

Fig. 13. Power spectrum of the residual echoes.

number of taps. It would be easily accomplished by increasing the number of the DSP boards.

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