AN OVERSAMPLING A-TO-D CONVERTER STRUCTURE FOR VLSI DIGITAL CODEC's

Akira YUKAWA , Rikio MARUTA and Kenji NAKAYAMA

NEC Corporation, Kawasaki, 213 Japan

ABSTRACT- Three kinds of encoder configurations, which include noise shaping, predictive and their combination forms, are investigated from LSI implementation points of view. A first order predictive encoder with first order noise shaping is chosen. A novel circuit configuration for the selected structure is proposed, which consists of a digital predictor with a capacitor array D-to-A converter, an operational amplifier and a comparator. The configuration can greatly decrease step unbalance effect, settling time and output voltage swing requirements for the operational amplifier, and the number of analog components. These features are essential in fine pattern LSI implementation. Capacitor fabrication error effects on the signal-to-noise ratio are numerically analyzed. A simplified decimation filter realization, which needs no high speed multiplier, is introduced.

INTRODUCTION

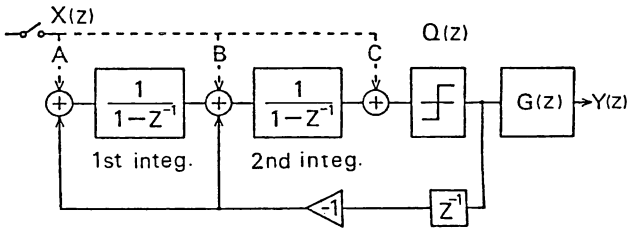
There are increasing demands for high quality analog to digital (A-to-D) converters for digital signal processing applications. Such high quality converters would be realized using VLSI technology. VLSI implementation requires low supply voltage operation and reduction of analog components. Conventional converters with a switched capacitor filter would not be suitable for VLSI implementation in view of requirements described above. Extensive efforts have been expended on oversampling schemes[1]-[4] to replace an analog filter by a digital filter. However, they were intended for nonlinear encoding, and are difficult to obtain high signal-to-noise ratio performance. Moreover, they all were designed for ±5 volt operation and it seems to be difficult to decrease the supply voltage. More attention should be paid to applicability to the VLSI fabrication process, as well as to improving performance.

In this paper, comparison among various encoder structures, which have a second order loop transfer function, is discussed. An encoder structure and its circuit configuration which seem to be most efficient for VLSI implementation are proposed. A possibility to realize a 14 bit or higher resolution is also investigated.

ENCODING STRUCTURES COMPARISON

There are three structures for oversampling encoders, namely predictive, noise shaping and their combination[5]. In designing these encoders, the order of loop transfer functions, the number of quantizer levels and the oversampling ratio must be determined. In view of simplicity for the quantizer itself and a decimation filter, it would be desirable to reduce the number of quantizer levels to two. Furthermore, taking stability and wide band applications into account, use of a second order loop transfer function would be desirable.

Fig. 1 shows a second order oversampling encoder. By feeding the input signal to node A, B or C, the encoder becomes a 2nd order noise shaping, a 1st order predictive with 1st order noise shaping or a 2nd order predictive encoder, respectively. Signal and noise transfer functions for each structure are shown in the same figure. Although each structure has no significant difference in the theoretical performance, differences in actual LSI implementational difficulties need to be thoroughly examined.



INPUT	G(z)	Y(z)
A	1	$X(z)+(1-Z^{-1})^2Q(z)$
B	$(1-Z^{-1})^{-1}$	$X(z)+(1-Z^{-1})Q(z)$
C	$(1-Z^{-1})^2$	$X(z)+Q(z)$

Fig. 1 Second order encoding structures.

Even in the fine pattern LSI technology, analog components are hard to scale down while keeping accuracies. In addition, noise induced in transistors would increase, thereby preventing the realization of high resolution A-to-D converters. Also due to decrease in break down voltages, a fine pattern LSI must operate at a low supply voltage. Therefore, analog signal processing should be replaced by digital signal processing and internal voltage swings in analog circuitry should be minimized. The above three structures are compared based on these properties, as well as on digital filter complexity, as shown in Table 1.

Of the three structures, structure A requires the largest dynamic range in integrators. The voltage swing in the second integrator exceeds four times of the input signal amplitude. The voltage swing in other two structures is nearly same to the input voltage amplitude.

Table 1 Comparison among three structures.

Structure	A	B	C
Internal voltage swing	large	small	small
Digital implementation	no	yes	yes
Active analog stage number	2	1	0
D/A converter bit number	1	6	12
Step unbalance sensitivity	large	small	small
Decimation filter complexity	○	Δ	X
High speed multiplier	no	yes	yes
Decimation filter attenuation	high	mid.	low

Although integrators in A must be realized with analog circuits, the first integrator in B and both integrators in C can be replaced by a digital integrator followed by a D-to-A converter. When this digital implementation is employed, the number of operational amplifiers, where analog signal has to pass through during one clock period, is 2, 1 and 0 for A, B and C, respectively. The number of bits required for the D-to-A converter is 1, 6 and 12 for A, B and C, respectively, when oversampling ratio is 128. A 6 bit D-to-A converter can be easily realized by a capacitor array. The digital integrator approach achieves a small chip area and low power consumption as compared to the analog integrator approach.

Voltage unbalance between positive and negative steps in the feedback path suffers signal-to-noise ratio performance, particularly in A. Use of the digital integrator can greatly decrease this step unbalance effect.

Multipliers operating at the oversampling frequency are basically required for the decimation filter in B and C, but not in A. Elimination of high speed multipliers for B will be discussed later.

Since the quantization noise spectrum is shaped by the second order differential function, the highest out-of-band attenuation is required for the decimation filter in A.

In summary, structure B is concluded the most attractive for fine pattern LSI implementation, provided that simplification on the decimation filter is accomplished.

ENCODER CIRCUIT CONFIGURATION

Fig. 2 shows the predictive encoder with noise shaping. The theoretical peak signal-to-noise ratio for this structure is expressed as,

$$S/N = \frac{3}{8}\left(\frac{fsh}{2\,fc}\right)^2\left(\frac{fsh}{fc}\right)\Big/\left(1-\frac{\sin(2\,fc/fsh)}{2\,fc/fsh}\right) \quad (1).$$

where fsh and fc are the oversampling frequency and signal bandwidth, respectively. Calculated theoretical peak signal-to-noise ratio performance is shown in Fig. 3, in terms of fsh, for the case of fc=4 kHz. The quantization level is also plotted in Fig. 3. The figure shows that 15 bit resolution is theoretically attainable by using 1.024 MHz oversampling frequency.

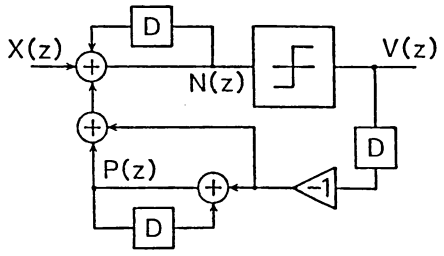


Fig. 2 1st order predictive encoder with 1st order noise shaping.

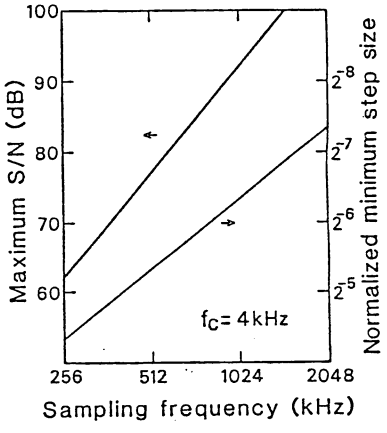


Fig. 3 Theoretical peak signal-to-noise ratio and step size.

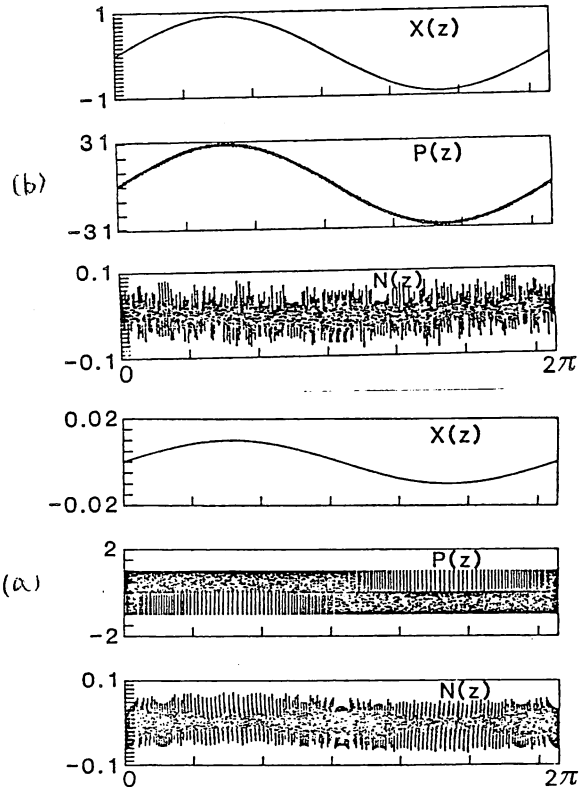


Fig. 4 Waveforms at various points in the encoder shown in Fig. 2. (a) Normalized input amplitude is 0.01. (b) Normalized input amplitude is 0.9.

Waveforms at various points in the encoder are shown in Figs. 4a and 4b for normalized input amplitudes 0.01 and 0.9, respectively. The comparator input amplitude is always kept small, independent of the input signal amplitude. Since the analog integrator output is kept small, the operational amplifier for this purpose can be easily realized with low power consumption.

For this structure, a novel circuit configuration, which requires only small amount of active analog components, is proposed here. It consists of a D-to-A converter, an operational amplifier and a comparator as shown in Fig. 5. The 6 bit D-to-A converter is realized by a 5 bit capacitor array for magnitude representation and polarity control gates. A direct path from the comparator output to the analog integrator input is also realized with an additional capacitor C placed in parallel with the D-to-A converter. The analog input signal is sampled and summed with the D-to-A output through the 32C capacitor, giving the resulting charge to the integrator. One notable feature of this configuration is that any analog voltage swing appears only at the integrator output. Furthermore, the voltage swing at the integrator output is very small.

Since step unbalance effect on signal-to-noi{e ratio depends on step size, this configuration can greatly decrease the effect, because the step size is reduced to 1/32 as compared to the case for noise shaping encoders without prediction.

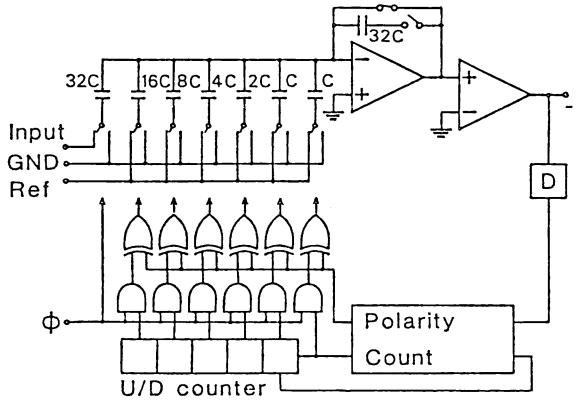


Fig. 5 Circuit configuration for the encoder structure in Fig. 2.

In LSI fabrication, capacitor ratio error is inevitable. This causes D-to-A converter inaccuracy and performance degradation. The effect of capacitor ratio error was analyzed by computer simulation. A capacitor array is constructed using unit capacitors. Deviation from the mean value in unit capacitance is inevitable in actual fabrication. Therefore, taking capacitor ratio errors for the capacitor array into account, Monte Carlo simulation was carried out to evaluate the degradation from the ideal performance as shown in Fig. 6. In this simulation, the standard deviation of the unit capacitance errors was set to 0.1% and the digital integrator dynamic range was forced to be limited within ±31/32. The thick solid line indicates the signal-to-noise ratio under no capacitance ratio error. Thin solid lines indicate results obtained from five trials. From Fig. 6, it is seen that more than 75 dB peak signal-to-noise ratio is obtained. The abrupt overload

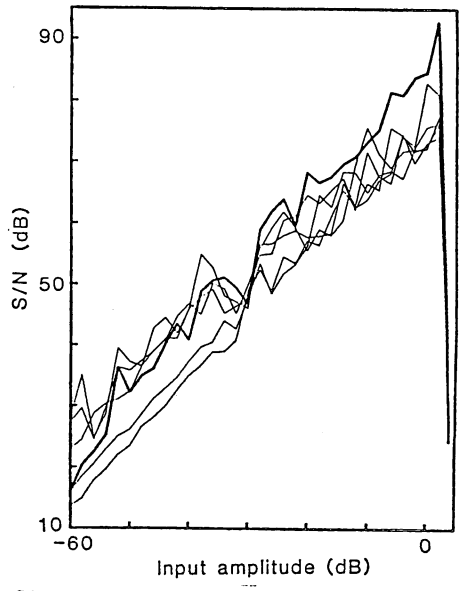


Fig. 6 Simulated signal-to-noise ratio performance taking into account of non-ideal D-to-A conversion due to capacitor ratio inaccuracy.

characteristics is due to the dynamic range limitation in the digital integrator. In order to attain a much higher resolution, increase in oversampling frequency or in capacitor ratio accuracy is required.

The features and simulation results described above justify the proposed circuit configuration.

DECIMATION FILTER STRUCTURE

The decimation filter is used as an antialiasing filter for sample rate reduction. In order to simplify its hardware, the filter is usually constructed as a cascaded form of a finite impulse response (FIR) filter and an infinite impulse response (IIR) filter. The FIR and the IIR sections operate at the oversampling frequency fsh and an intermediate frequency fsm, respectively. The IIR section output is finally sampled at the baseband sampling frequency fsl.

Since a predictive encoder requires a digital integrator G(z) at the output stage, as shown Fig. 1, the FIR filter input is no longer a single bit signal. Thus, in general, high speed multipliers are required to implement the FIR filter. In order to avoid this, the digital integrator G(z) is reconstructed as,

$$G(z)=\frac{1}{1-Z^{-1}}=\frac{1+Z^{-1}+Z^{-2}+\cdots+Z^{-N+1}}{1-Z^{-N}} \qquad (2).$$

$$Z=\exp(j\omega T)\ ,\ T=1/fsh\ .$$

The numerator in Eq. (2) is combined with the FIR filter transfer function, and the denominator is included in the transfer function of the IIR filter.

Letting F1(z) be an FIR filter transfer function, the modified form becomes

$$\tilde{F}_1(z)=(1+Z^{-1}+Z^{-2}+\cdots+Z^{-N+1}) \qquad (3,a),$$

$$=\sum_{n=0}^{m-1}\tilde{h}_n Z^{-n} \qquad (3,b).$$

Since the input to the modified FIR filter is a single bit signal, its hardware can now be easily constructed using a read only memory (ROM), an accumulator and registers as shown in Fig. 7. This circuit configuration can easily accomplish high speed filtering, and does not impose any constraint on the filter coefficient values, $\{\tilde{h}_n\}$.

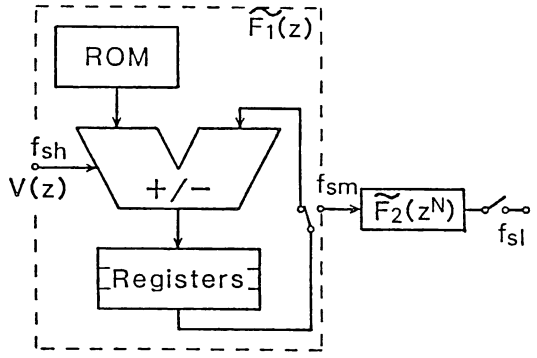


Fig. 7 Decimation filter structure.

Letting $F2(z^N)$ be a transfer function of an original IIR filter, the modified form including the denominator of Eq. (3) becomes,

$$\tilde{F}_2(z^N) = \frac{1}{1-z^{-N}} F_2(z^N), \quad fsm=fsh/N \qquad (4).$$

In order to eliminate a low frequency noise, $F2(z^N)$ usually has at least a pair of pole and zero at $\omega T=0$. Letting

$$F_2(z^N) = \frac{1}{1-rz^{-N}} F'_2(z^N), \quad 0 < r < 1 \qquad (5),$$

the modified form is rewritten as,

$$\tilde{F}_2(z^N) = \frac{1}{1-rz^{-N}} F'_2(z^N) \qquad (6).$$

This modification implies that $F2(z^N)$ is obtained by removing the zero located on the unit circle at $\omega T=0$ in the original transfer function $F2(z^N)$.

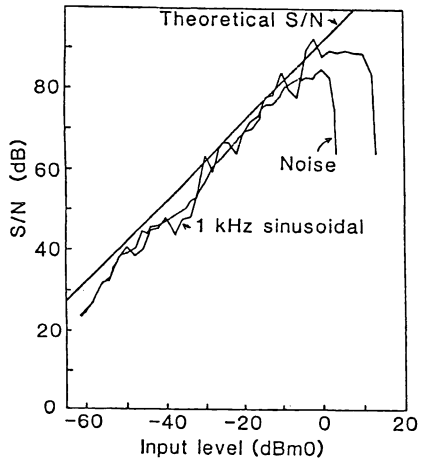


Fig. 8 Signal-to-noise ratio performance including finite stopband attenuation effect for 1 kHz sinusoidal and random noise inputs.

SIMULATION

The proposed encoder including the decimation filter was analyzed through computer simulation. Signal-to-noise ratio performance was analyzed for 1 kHz sinusoidal and random noise inputs, as shown in Fig. 8. The encoder overload point was set to 3.17 dBm0 at 3.4 kHz. The random noise is a low pass signal whose spectrum has a 6 dB/octave slope and extends up to 15 kHz. The decimation filter is designed according to the previous discussion. A 128 tap FIR filter and an 8th order IIR filter are used. The overload level is mainly determined by slope overload at the predictor.

CONCLUSION

Comparison between several oversampling encoder structure has been discussed, and a 1st order predictive encoder with 1st order noise shaping has been chosen. A novel circuit configuration for the selected structure has been proposed, which is constructed with a digital predictor followed by a switched capacitor D-to-A, an operational amplifier and a comparator. It has features essential to fine pattern LSI implementation. Furthermore, taking the simplified decimation filter structure into account, the proposed encoder structure is confirmed to be most efficient for VLSI implementation.

ACKNOWLEDGMENT

The authors would like to thank their colleagues for useful discussions and helps in computer simulation. The authors also appreciate encouragements given by Drs. Y. Okuto, H. Goto and H. Sakuma.

Reference

[1] B.A. Wooly and J.L. Henry, "An Integrated per-channel PCM encoder based on Interpolation," IEEE J. Solid-State Circuits, vol. SC-14, pp14-20, 1979.
[2] T. Misawa et al, "Single-chip per Channel Codec with Filters Utilizing ΣΔ-Moduration," IEEE J. Solid-State Circuits, vol. SC-16, pp. 333-341, 1981.
[3] D. Vogel and W. Pribyl, "CMOS Digital Signal-Processing Codec Filter with High Performance and Flexibility," ESSCIRC '84 Conference Records, pp. 43-46, 1984.
[4] B. P. Agrawel and K. Senoi, "Design Methodology for ΔM," IEEE Trans. Communications, vol. COM-31, pp. 360-370, 1983.
[5] S. T. Tewksbury and R. W. Harrock, "Oversampled, Linear Predictive and Noise-Shaping Coder of N>1," IEEE Trans. Circuit and Systems, vol. CAS-25, pp. 436-447,1978.