A PERSONAL TRANSCEIVER BASEBAND LSI USING SWITCHED CAPACITOR CIRCUIT TECHNIQUES

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ABSTRACT

A single chip baseband LSI for personal transceivers is presented. This LSI consists of a digital section, which includes a 145 MHz phase locked loop and others, and an analog section. The analog section includes various filters with 26th-total order, limiter, integrator and differentiator. In order to achieve significant reductions in layout area and power dissipation, switched capacitor (SC) circuit techniques are employed. The filters are synthesized with low sensitivity LC ladder SC filters. Capacitor values of the SC filters are rounded off into integer values, and are discretely optimized. These techniques can allow us to use a small unit capacitor. A range of capacitor ratios is compressed through scaling up small capacitor values by dividing their voltages. An LSI was fabricated using 3 μm CMOS technology. Experimental results are very close to designed performances.

INTRODUCTION

Personal transceivers, which can be used as mobile transceivers, have been required to be miniaturized and to have a low power dissipation. One hopeful approach to meeting this purpose is to implement a baseband filter block on a monolithic MOS circuit.

This paper presents a single chip baseband LSI for personal transceivers using 3 μm CMOS technology, as well as switched capacitor circuit techniques.

SYSTEM DESCRIPTION

Figure 1 shows a block diagram for the baseband system to be implemented on a single-chip monolithic MOS circuit. This block includes a digital section and an analog section consisting of transmitter and receiver. These blocks have been realized on separated monolithic or hybrid integrated circuits up to now (ref 1).

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The digital section consists of 145 MHz phase locked loop, programmable frequency divider, fixed frequency divider and phase detector.

The analog section contains various kinds of filters, integrator, differentiator and limiter. These functional blocks are synthesized using switched capacitor (SC) circuits in order to accomplish high level performances on monolithic MOS circuits with a small layout area and with a low power dissipation (ref 2). Since SC circuits are basically analog sampled data systems, prefilters and post-filters, which are synthesized by RC active filters, are further required for anti-aliasing and signal smoothing.

The conventional circuit configurations using bipolar transistors for the digital section can be easily transformed into the corresponding CMOS circuits. The high speed performances can be basically achieved by employing fine CMOS technology. Therefore, in the following sections, this paper places stress on design techniques and LSI implementation for the analog section.

ANALOG SECTION

Filters

In order to satisfy strict tolerances for passband ripples and to relax the requirement for capacitor ratio accuracy, LC ladder SC filters (SCFs) are employed. Figures 2(a) and (b) show a prototype LC ladder highpass filter (HPF) and the simulated SC HPF, respectively. Passband ripple deviations, in the worst case, with 1 percent capacitor ratio errors, are less than 20 percent of the tolerances for both the transmitter and receiver.

Since a range of capacitor ratios is proportional to a ratio of sampling and cutoff frequencies, it becomes very large in the HPF whose sampling and cutoff frequencies are 100 kHz and 230 Hz, respectively. In order to compress this range, small capacitor values are scaled up by dividing their voltages with capacitive divider circuits, as shown in Fig. 2(b) with dashed lines. After the capacitor value scaling, the total amount of capacitor values in the HPF is reduced to 28 percent of that before scaling.

As is well known, SCF performances are determined by capacitor ratios. In order to attain high capacitor ratio accurracy with small capacitors on monolithic MOS circuits, it is necessary to realize arbitrary capacitors using a plural number of the same unit capacitors. For this purpose, the capacitor values which are initially obtained from the prototype LC ladder filters are rounded off into integer values, and effects of roundoff errors, as well as the doubly resistive termination errors on filter responses, are minimized by automatically searching for optimum discrete value capacitors around the initial value (ref 3).

By combining the low sensitivity filter structures and the discrete value capacitors, the unit capacitor value can be sufficiently reduced. In the developed LSI, 0.2 pF and 0.1 pF unit capacitors are employed for voice band and data band SCFs, respectively. The compressed capacitor ratio ranges and the above mentioned small unit capacitors can make SCFs have a small occupied area and, at the same time, a low power dissipation with light capacitive loads for operational amplifiers.

LPFs1 and 3 are 4th and 2nd-order weighted Chebyshev lowpass filters, whose cutoff frequencies are 3 and 5 kHz, respectively. LPFs2 and 4 are 2nd-order Butterworth lowpass filters having 500 and 300 Hz cutoff frequencies, respectively. The integrator and differentiator are synthesized by 1st-order SC circuits, whose transfer functions are approximated through an iterative approximation method.

Limiter

Figure 3 shows a limiter circuit block diagram. A boundary voltage circuit and a comparator are synthesized with SC circuits. A selector contains three SC circuits, which form the input stage for LPF1. One of three SC circuits is selected to operate normally. The other SC circuits are controlled to hold the charges for their input voltages. The comparator output has three states, corresponding to $V_{in} < -1V$, $-1V \leq V_{in} \leq 1V$ and $1V < V_{in}$. According to these states, the controller generates clock signals for the SC circuits in the selector.

LSI IMPLEMENTATION

The transceiver baseband LSI was fabricated on a single chip monolithic MOS circuit using 3 μm CMOS technology. A chip photograph, showing a part of the analog section including SCFs and other SC circuits, is given in Fig. 4. The area and power dissipation for this block are 7.1 mm^2 and 37.5 mW in an active mode, respectively. About 74 percent of the power dissipation can be saved during a power down mode. The analog section further has a 9.3 mm^2 area and a 14.6 mW power dissipation for the RC active filters.

Figures 5(a) and (b) show measured frequency responses for the transmitter and receiver, respectively. These results are mostly the same as the designed performances, and satisfy the strict specifications for the passband (0.3-3 kHz) ripples by a 50 percent margin.

The measured output level in terms of the input for the limiter is given in Fig. 6, and prove precise response performance.

CONCLUSION

A single chip baseband LSI for personal transceivers was fabricated on the 3 μm monolithic CMOS circuit. The experimental results were very close to the designed performances. The developed LSI is now being evaluated through field tests, and demonstrates good performances.

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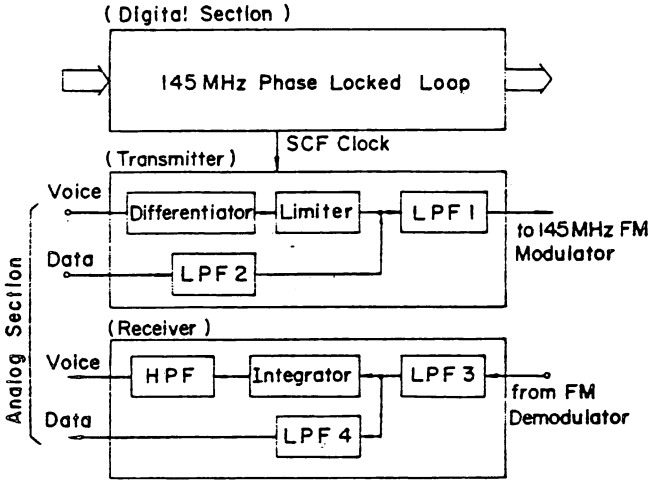


Fig. 1. Block diagram of personal transceiver baseband LSI.

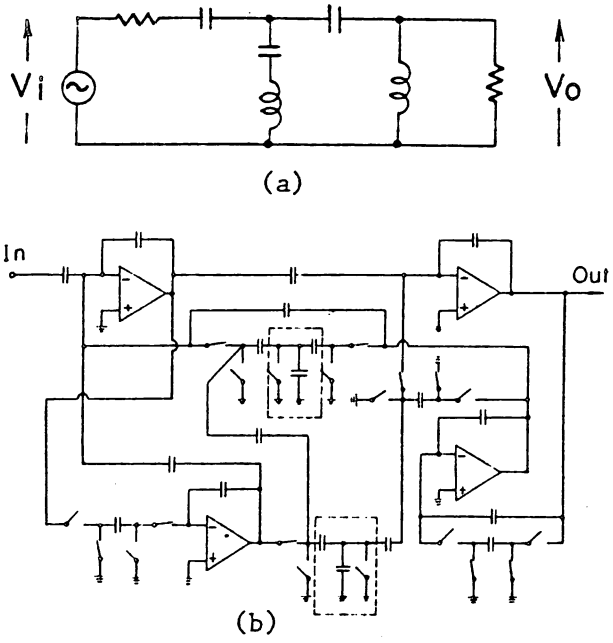


Fig. 2. (a) Prototype LC ladder highpass filter. (b) Simulated SC highpass filter. Capacitive dividers are enclosed with dashed lines.

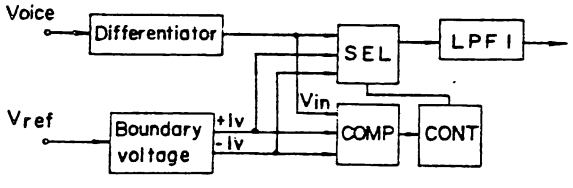


Fig. 3. Limiter circuit.

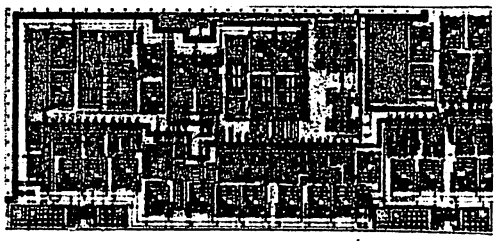
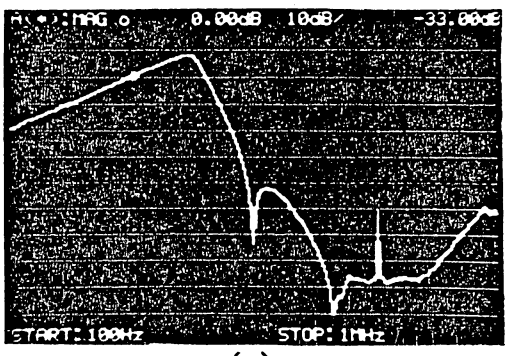
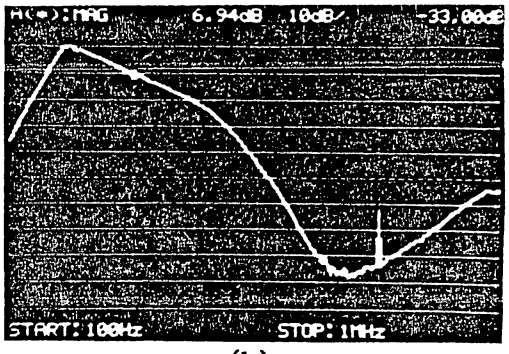


Fig. 4. Chip photograph of analog section including SCFs and other SC circuits.



(a)



(b)

Fig. 5. Measured amplitude responses. (a) Transmitter. (b) Receiver.

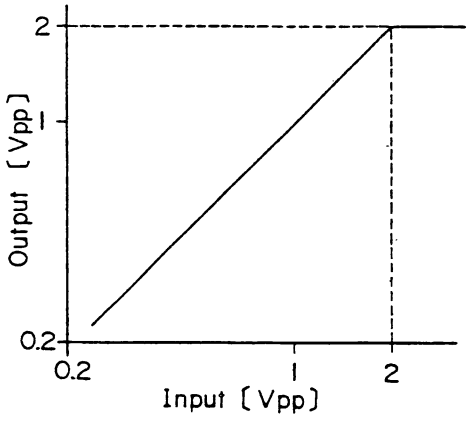


Fig. 6. Limiter output level (Vpp) in terms of the input level (Vpp).