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Present and Future Trends in Integrated Analog Signal Processing Circuits

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SUMMARY Analog signal processing is important for the following reasons. There exist many analog environments, and integrated analog circuits have several advantages over digital circuits. On the other hand, a digital approach can provide another features, such as accurate operation and programmability. Therefore, both circuits are effectively combined, resulting in high performance LSIs. This tutorial paper provides an overview for the recent and future trends in design and applications of integrated analog signal processing circuits. First, design techniques are reviewed for operational amplifier (Op-Amp), monolithic bipolar active RC circuits, switched-capacitor (SC) circuits, continuous-time MOS circuits, and analog-to-digital converter (ADC). High frequency filter realization, up to 100 MHz, has been tried by bipolar active RC circuits and GaAs circuits. Improved design techniques for SC circuits have been proposed. They include noise cancellation and building blocks with reduced sensitivity to nonideal Op-Amp performance. In order to overcome some SC circuit drawbacks due to a sampled data circuit, continuous-time MOS circuits have been proposed. Successful results have been obtained by using an automatic tuning method. A multi-stage noise shaping ADC is very useful to integrate an accurate ADC. A high signal-to-noise ratio (SNR), more than 91 dB, was obtained by the three-stage ADC, which can be applied to digital audio systems. Automatic design and fabrication processes are also important aspects. Silicon compilers for SC circuits are overviewed. Systematic design rule, by which a globally optimum solution can be obtained, requires further investigation. A mixed analog/digital master slice LSI has been proposed to simplify an LSI customizing process. A voice-band MODEM LSI has been developed, resulting in good filter responses and SNR. Finally, promising applications of integrated analog circuits are briefly reviewed. Analog circuits are superior to a digital version in operating speed, power dissipation and integration density. In actuality, however, both approaches will be combined, resulting in mixed analog/digital LSIs where both circuits supplement each other's excellent features and negate drawbacks.

1. Introduction

Analog signal processing is important technology for many reasons. First, there exist analog signals in many cases. For instance, signal sources, transmitted signal over line, and perceptible signal by human are all analog signals. Furthermore, integrated analog circuits have several advantages over digital circuits, such as high speed operation, low power dissipation, and high integration density.

Design technology for integrated analog circuits has made a great progress during the recent decade. They include monolithic bipolar active RC circuits, switched-capacitor (SC) circuits, and continuous-time MOS circuits. High frequency filter realization, up to 100 MHz, has been tried by bipolar active RC circuits and GaAs SC circuits. Several design techniques to reduce noise and power dissipation in SC circuits have been continued. Application field of integrated analog circuits spreads from communication and speech processing to video signal processing, medical systems and nueral networks[1]-[3].

Design and fabrication processes for integrated analog circuits are complicated and usually require highly sophisticated know-how. For this reason, their applications are rather limited. In order to overcome this problem, automatic design tools, such as silicon compilers, are very important. Reduction in LSI fabrication cost and term is also an important aspect. Analog master slice and programmable analog circuits have been developed for this purpose.

This paper provides a tutorial review for recent and future trends in design and applications of integrated analog signal processing circuits. First, design techniques are reviewed for operational amplifiers (Op-Amps), bipolar active RC circuits, SC circuits, CMOS continuous-time circuits, and analog-to-digital converter. Stress will be placed on how to achieve high speed operation, high accuracy, low power dissipation, etc. Silicon compilers are briefly overviewed mainly for SC circuits. As a simple LSI customizing process, analog master slice and programmable analog circuits are briefly reviewed. Finally, promising applications in the future are described taking features of the integrated analog circuits into account.

2. Integrated Analog Circuits

2.1 Performance and Application

Figure 1 shows relations between element counts and signal frequency of analog LSIs and mixed analog/digital LSIs[3]. Digital signal processing LSIs are also included in this figure. Analog circuits are mainly used in

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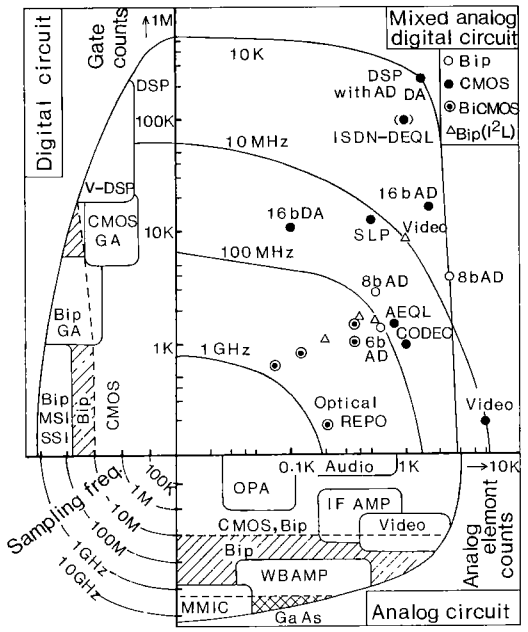

Fig. 1 Relations between element counts and signal frequency in analog LSI and mixed analog/digital LSI.

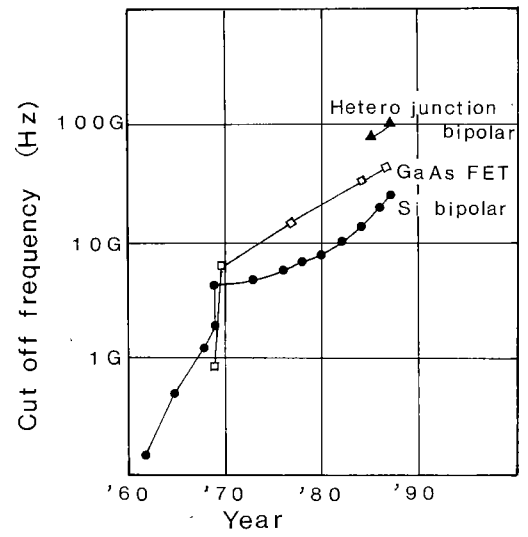

Fig. 2 Progress of f_T in ultra-high speed devices.

the frequency band ranging from voice to video signal frequencies. Conventional bipolar circuits are mainly used in this field. Furthermore, conventional analog LSIs have been gradually replaced by a mixed analog/digital LSIs from the low frequency region in order to achieve high performance.

In a higher frequency domain than the above, a several GHz wide-band amplifier and a narrow-band MMIC with over 20 GHz have been developed. Figure 2 shows the progress of f_T in ultra-high speed devices. As speed of Si bipolar approaching the upper limit, compound semiconductor devices, such as GaAsFET,

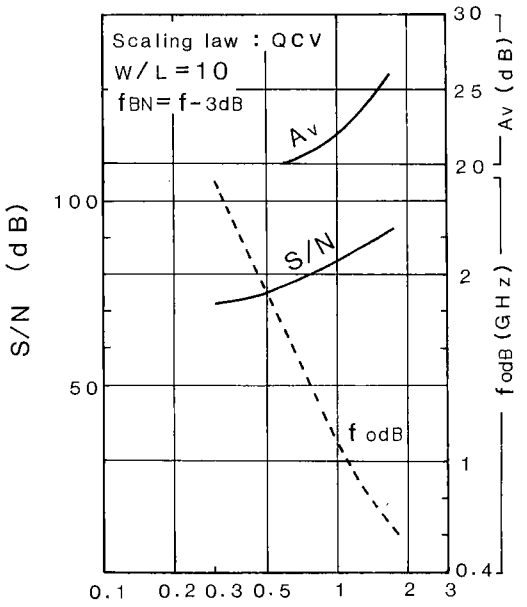

Fig. 3 Relations between analog circuit performance and effective channel length (Simulated).

AlGaAs-GaAs hetero-junction bipolar, and high electron-mobility transistor, have become important. A 100 GHz f_T has been obtained as a top data. These devices are mainly applied to high speed and small size analog circuits.

Performance and integration density for digital circuits can be improved by device scalings. On the contrary, sufficient reduction in a chip area and power dissipation for analog circuits cannot be expected. Although bandwidth of Op-Amp is increased by a scaling law, a DC gain and a signal-to-noise ratio (SNR) are, however, decreased. Figure 3 shows a relation between analog circuit performance and an effective channel lengths[4].

Bipolar transistors are useful to achieve high accuracy, low noise, and wide-band operation in analog circuits. Mixed bipolar and CMOS devices, i.e., BiCMOS technology, have been developed. Furthermore, high breakdown voltage device is required for analog circuits. Dielectric isolated bipolar device is combined for this purpose.

2.2 Operational Amplifiers

Figure 4 shows performance of monolithic Op-Amps. Developement of Op-Amp is directed towards both achieving high speed and high accuracy performance[3].

To achieve highly accurate Op-Amps, refinement of bipolar circuits and CMOS chopper stabilized circuits are employed. A voltage gain and a common mode rejection ratio (CMRR) can be improved up to 120 dB. In order to obtain high speed Op-Amps, high slew-rate Op-Amps using FET and MOS device as an input stage

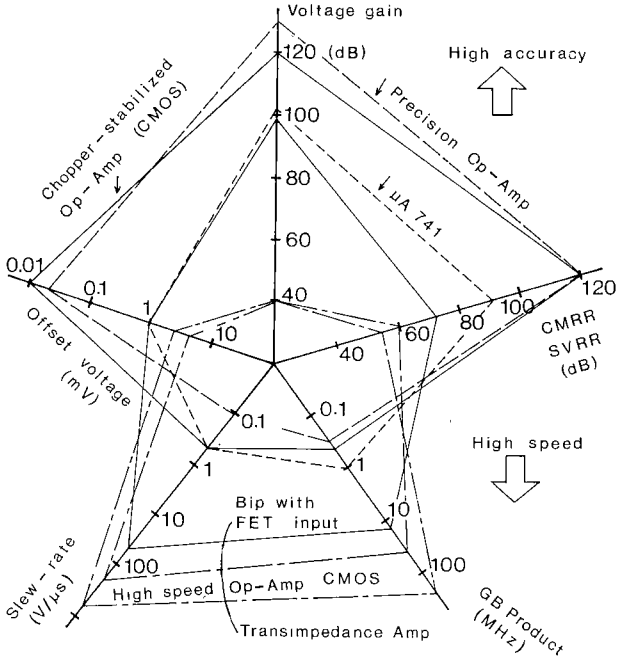

Fig. 4 Performance of monolithic operational amplifiers.

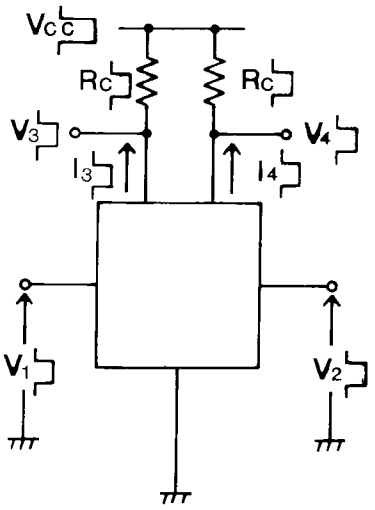

Fig. 5 Symmetric differential balance-unbalance converter with load resistors.

and wide-band Op-Amps made by transconductance amplifier have been developed. From Fig. 4, it is recognized that simultaneous improvement in both speed and accuracy seems to be difficult.

3. Active RC Circuits

3.1 Bipolar Active RC Circuits

Bipolar devices are suitable for high frequency, low noise filter realization compaired with MOS devices[1].

3.1.1 Balance-Unbalance Converter

A balanced circuit requires a relatively large number of elements. However, it has the following features : reduction in parasitic capacitor effects, even-order nonlinieality cancellation, and gyrator realization. These features are suited to develop high-frequency active RC filters. Furthermore, an LC ladder filter can be simulated using the gyrator.

Since the input signal is usually unbalanced signal, an unbalance-balance converter is necessary. A symmetric differential circuits, shown in Fig. 5, is employed for this purpose. In this circuit , resistive loads are extracted. In order to obtain high gain over a wide frequency band and to increase CMRR, a balanced negative impedance converter (NIC) can be employed in parallel with the output port. This structure is directly applied to designing a differential integrator used in a leap-frog active RC filter.

3.1.2 Video-Band Monolithic Filters

A differential integrator constructed with NIC has good CMRR and is suited to high-frequency filter realization. A monolithic third-order leap-frog lowpass filter with 5 MHz cutoff frequency has been fabricated using a 3 μm bipolar process[5] with a 5 GHz f_T. Measured data are slightly different from the designed, due to element value deviation and wire parasitic capacitors.

3.1.3 VHF-Band Monolithic Filters

A balanced NIC seems to be the most hopeful functional element in VHF-band active RC filters. One example is described here. Figure 6(a) shows a prototype 3rd-order LCR filter. A floating inductor L can be replaced by a pair of gyrators and a grounded capacitor as shown in Fig. 6(b). Furthermore, each gyrator is replaced by the balanced NICs and resistors as shown in Fig. 6(c)[6]. An LSI was fabricated using the same process as the before-mentioned leap-frog filter. Simulation (dot-dash-curve) and experimental (solid and broken curves) results are shown in Fig. 7. Although a cutoff frequency shifts from 100 MHz to 70 MHz, this result demonstrates the possibility of VHF-band monolithic active RC filter.

3.2 CMOS Active RC Circuits

As will be described in the next section, an SC circuit is a sampled-data circuit, and anti-aliasing and smoothing filters are required. They are usually constructed with active RC filters, which occupy a large

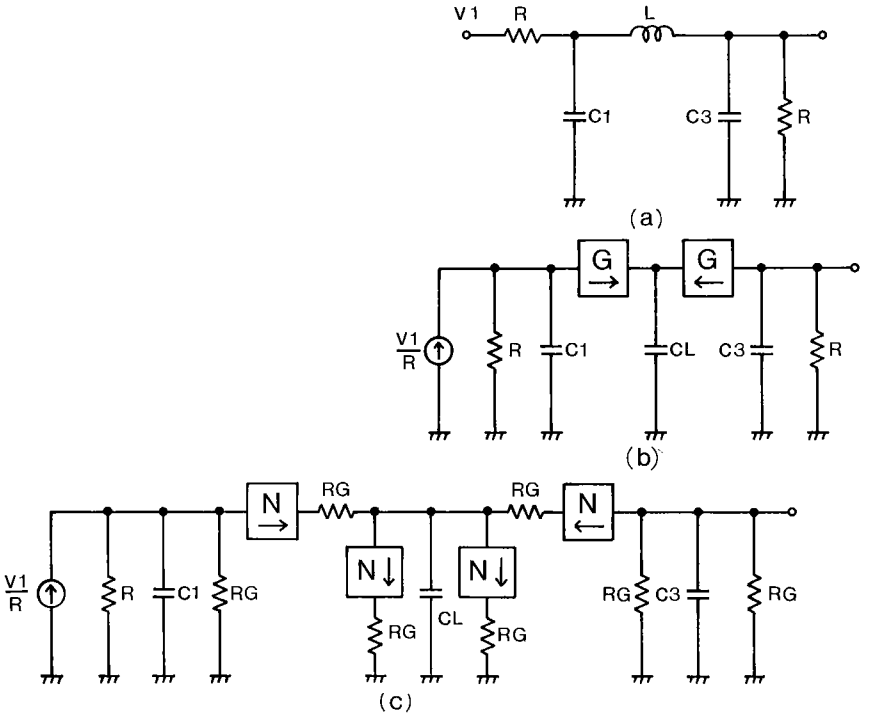

Fig. 6 Realization of 100 MHz third-order lowpass filter.
(a) Prototype LCR filter.
(b) Simulation with gyrators.
(c) Gyrators are replaced by NIC's.

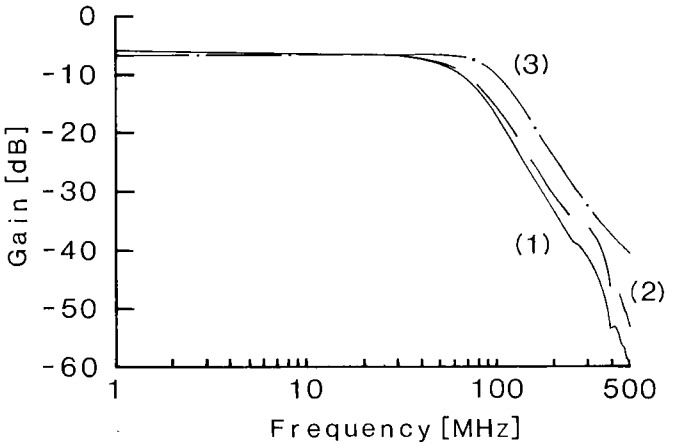

Fig. 7 Simulated (3) and experimental (1), (2) results.

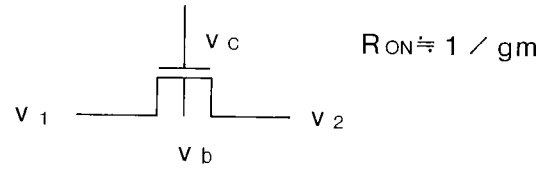

Fig. 8 MOSFET resistor.

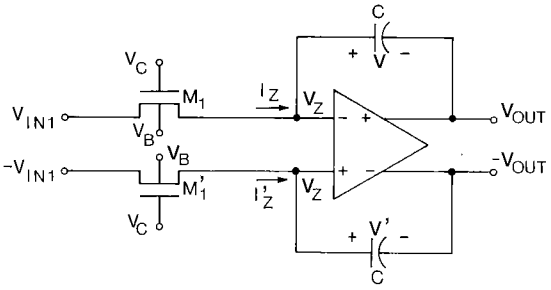

Fig. 9 Input-output balanced MOSFET-C integrator.

chip area. Furthermore, a clock driver is necessary. Another problem is noise. Wideband thermal noise and digital noise are shifted into a passband by sampling. In order to solve these problems, continuous-time CMOS circuits have been developed.

A resistor is realized by using MOS transistor as shown in Fig. 8. A resitor is given by $R_{on}=1/g_m$. In the MOS transistor, the current is expressed as

$$I_D=K[a_1(V_1-V_2)+a_2(V_1^2-V_2^2)+a_3(V_1^3-V_2^3)+\cdots] \quad (1)$$

where the coefficients a_1, a_2, a_n are given by

$$a_1=2(V_C-V_T) \quad (2\,a)$$

$$a_2=-\left(1+\frac{r}{2-V_B+\phi_B}\right) \quad (2\,b)$$

$$a_n=-A(n)(-V_B+\phi_B)^{-(2n-3)/2}, \quad n\geq 3 \quad (2\,c)$$

$$V_T=V_{FB}+\phi_B+r\sqrt{-V_B+\phi_B} \quad (2\,d)$$

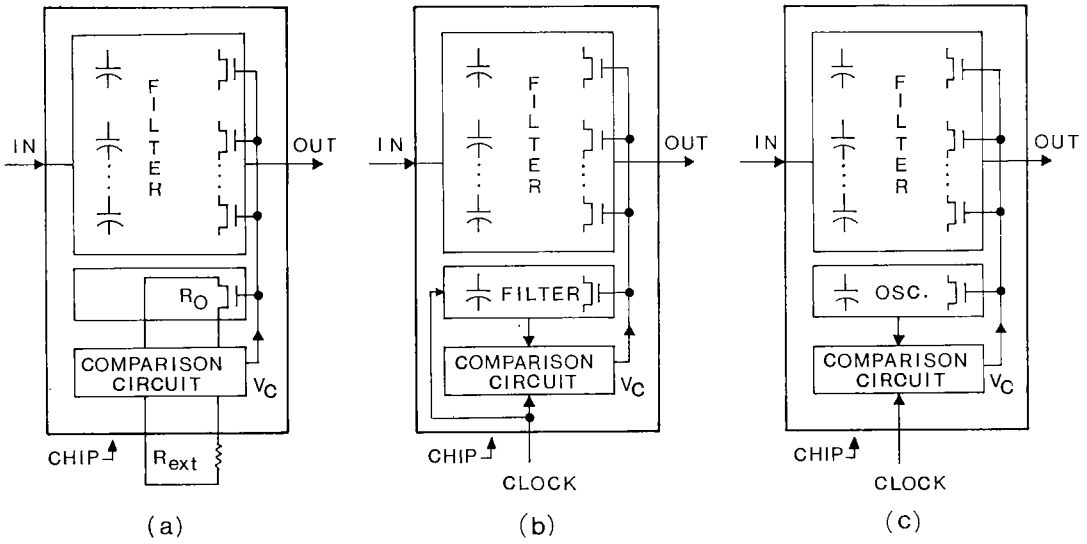

Fig. 10 On-chip automatic indirect tuning schemes.
(a) With an external resistor as reference.
(b) With a clock signal as reference and a voltage-controlled filter in the tuning loop.
(c) With a clock signal as reference and a voltage-controlled oscillator in the tuning loop.

$$r=\frac{1}{C'_{ox}}(2qN_A\varepsilon_S)^{1/2} \tag{2e}$$

$$K=\frac{1}{2}\mu C'_{ox}\frac{W}{L} \tag{2f}$$

A problem in this approach is nolinearlity as shown in Eq. (1). Even-order distortion can be cancelled by using a balanced circuit. An example of a balanced integrator is shown in Fig. 9[7].

A transfer function for an active RC circuit is determined by absolute element values. Therefore, an automatic tuning method becomes very important. Several methods have been reported as shown in Fig. 10[8].

A fifth-order elliptic lowpass filter with 0.05 dB passband ripple and 3.4 kHz cutoff frequency has been implemented in a 3.5 μm CMOS technology[9]. A phase locked loop control system, fabricated on the same chip, automatically references the frequency response of the filter to an external fixed clock frequency. The cutoff frequency was measured to vary less than 0.1 percent for a temperature range of 0–85°C. The measured dynamic range is approximately 100 dB with ±5 V power supplies.

4. Switched-Capacitor Circuits

4.1 CMOS SC Circuits

An SC circuit consists of switchs, capacitors and Op-Amps, which can be integrated on an MOS-IC. Therefore, SC circuits are suitable for mixed analog/digital LSIs. SC circuit characteristics are determined by capacitance ratios. This can provide highly accurate filter responses and a small chip area. Furthermore, a time division multiplexed (TDM) structure and programmability are also possible in SC circuits.

Basic design techniques have been mostly developed during the decade from 1975. Current research objectives mainly include SC circuits synthesis insensitive to nonideal element effects, a globally optimum design rule, and SC silicon compilers.

4.1.1 Noise Reduction

DC offset is caused by Op-Amps and clock feedthrough. Several DC offset cancellation methods have been proposed. One of them is to extract the output DC offset through an integrator, and negatively feedback it into an SC circuit[10]. In ping-pong data transmission systems, a line equalizer is used only during the receiving mode. Therefore, the output DC offset can be detected during the transmitting mode, and is stored in a capacitor. It is substracted from the signal during the active mode[11]. Another method is to use an offset insensitive integrator[12].

$1/f$ noise is caused by Op-Amps. A large input transistor pair, chopper stabilized differential SC circuits[13], and correlated double sampling method[14] are useful to reduce $1/f$ noise. These techniques, however, need a relatively large chip area. TDM realization of differential SC circuits[15], and a low-frequency noise insensitive integrator[16] can save chip area.

Power supply rejection ratio (PSRR) improvement is also an important aspect. Since power supply noise is

Table 1 kT/C noise for different capacitor values.

KT/C Noise	
C(pF)	$\sqrt{(KT/C)}$(μV)
100.0	6.4
10.0	20.2
1.0	64.0
0.1	202.0

a common mode, it can be cancelled by using differential SC circuits. PSRR is improved from 20-40 dB in single-ended SC circuits up to 50-60 dB in differential SC circuits. In order to improve PSRR in a single-ended SC circuit, a new clock buffer has been proposed[17].

4.1.2 High Integration Density

A switch and an Op-Amp can be miniaturized through fine-pattern technology and scaling laws. An Op-Amp was designed on a 75×90 μm (=6750 μm^2) chip area using a 1.5-μm CMOS process[18]. Recent process technology is approaching 0.7-0.8-μm rules for memory fabrication. Therefore, a design process seems to be scaled down to a 0.5-μm rule. In that case, an Op-Amp chip area could be dereased to 750 μm^2.

When a fine-pattern technique is employed, however, careful attention should be given to overcome the following problems: low breakdown voltage, electromigration effects, and accuracy limits, etc.

On the contrary, capacitor size reduction is bounded by specifications for the output noise. Thermal noise produced in an FET switch is bandlimited through an RC lowpass filter consisting of a sampling capacitor C and a resistor of an FET switch. The total thermal noise in the passband is given by kT/C, where k and T are Boltzmann's constant and absolute temperature, respectively. Since the total noise is inversely proportional to the sampling capacitance C, it cannot be sufficiently decreased. Numerical examples for the kT/C noise are listed in the Table 1[19]. From these results, the sampling capacitance is desirable to be more than 0.2pF, having a 300 μm^2 chip area.

Furthermore, clock feedthrough and power supply noise are induced through parasitic capacitors. The output noise is proportional to a ratio of parasitic capacitance and integrating capacitance. For instance, in a 3-μm CMOS process, parasitic capacitances are about 0.001 - 0.005 pF. Therefore, the integrating capacitance should be more than 1-2 pF. A capacitor surface area can be saved by reducing the dielectric thickness. This approach has also the lower limit due to breakdown voltage reduction.

Taking the above relations into account, capacitor size cannot be sufficiently reduced. In the case of a first-order SC circuit, whose total capacitance is 2 pF(=3000 μm^2), and a submicron design rule is assumed, 80 percent of a chip area is occupied by capacitors.

4.1.3 High Speed Operation

Operating speed is mainly determined by settling time of an Op-Amp. A single-stage cascode configuration exhibits faster settling behavior than a two-stage configuration. Assuming a single-pole transfer function and high slew-rate, the settling time is determined by a unity-gain bandwidth $\omega_t=g_m/C_L$, where C_L is a capacitive load and g_m is a transconductance. Since g_m is proportional to W/L and $1/t_{ox}$, it is possible to design g_m to be sufficiently large by scaling laws or fine-pattern technology. Therefore, ω_t can be increased by g_m, even though C_L has some lower limit.

4.1.4 Low Power Dissipation

Power dissipation can be decreased by relaxing requirements for Op-Amp performance. Minimum requirements for DC gain, bandwidth and a slew-rate have been determined based on the relation between finite Op-Amp characteristics and filter responses. A 4th-order elliptic SC filter with 190 μW power dissipation has been developed[20]. A cutoff frequency is 5 kHz, and a power supplies are ±2.5 V. The building blocks with reduced sensitivity to finite Op-Amp characteristics are also useful for this purpose.

When plural integrators are connected through capacitors in a serial path or in a loop, a total settling time becomes larger than that for a single integrator. In this case, a faster settling time is required for a single Op-Amp, resulting in high power dissipation. Such a long capacitive path or loop can be shortened by shifting clock phase by a half clock period and by inserting a switch in a coupling capacitor path[21].

Power dissipation in SC circuits is classified into two categories: static power that consumed by DC bias current in Op-Amps, and dynamic power that consumed during charge and discharge periods. Although the static power dissipation is still dominant, there is much room for drastically saving this dissipation. The essentially required minimum power dissipation is given by the dynamic power dissipation. Class B or dynamic amplifier schematics are useful for this purpose[22],[23].

The theoretical dynamic power dissipation is given by $P_d=8fC_IV_s^2$ for a first-order SC circuit[24]. f is an input signal frequency, C_I is an integrating capacitance, and V_s is supply voltage. Since V_s is usually determined by another requirements, such as a signal dynamic range and SNR, P_d is mainly determined by C_I which has some lower limit. However, the dynamic power dissipation is still sufficiently smaller than the static one. For example, assuming $f=500$ kHz and $C_I=5$ pF, P_d becomes 0.5 mW with a single +5 V supply. This indicates very low power dissipation could be possible.

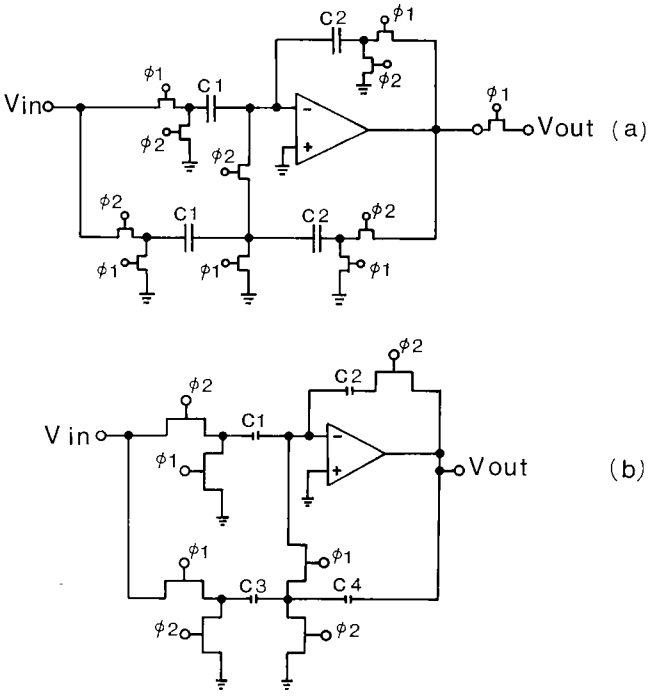

Fig. 11 SC building blocks with reduced sensitivity to DC offset and finite DC gain of OP-Amp.
(a) Gain stage. (b) Inverting integrator.

4.2 GaAs MESFET SC Circuits

GaAs MESFET technology has been applied to high frequency SC circuits. GaAs Op-Amps have low DC gain and high DC offset voltage[25]. In order to suppress these nonideal effects, a low sensitivity gain stage and an improved gain-compensated inverting integrator have been developed[16]. Their circuit diagrams are shown in Fig. 11. A transfer function for the gain stage is given by

$$H(z)=-\frac{C_1}{C_2}\frac{1+\frac{x}{1+2x}(1-z^{-1})}{(1+x)[1-xz^{-1}/(1+2x)]}$$

$$x=(1+C_1/C_2)/A$$

A is a DC gain. When A is relatively large, finite DC gain effect, that is x, can be neglected. 10 MHz-band SC filters drived by a 100 MHz clock frequency have been reported.

Generally speaking, low amplifier gain is often the result of wide bandwidth design, maintaining the same power dissipation. The above proposed SC building blocks are also useful in this case.

5. Analog-Digital Converters

5.1 Conversion Schematics

An analog-to-digital converter (ADC) is an important analog function block. Figure 12 summarize schematics, resolution and conversion rate[3]. For high-frequency application, a parallel method has been used. A 400 Msps ADC with 8 bits, and a 2 Gsps ADC with 6 bits have been achieved[27],[28]. Highly accurate ADCs are effectively realized using an oversampling method. A 48 ksps ADC with 16 bits has been developed[29].

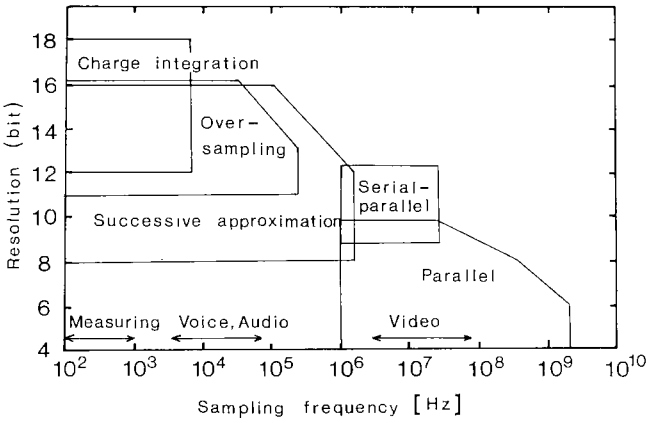

Fig. 12 Performance of integrated analog-to-digital converters in terms of resolution and conversion rate.

5.2 High Speed Conversion

A paralell ADC consists of the same number of comparators as quantization levels, and converts analog signal to digital signal within a clock period. Therefore, a sample-hold circuit is not necessary, with which highly accurate conversion is rather difficult. A conversion rate is determined by a comparator response time. Conversion accuracy is dependent on quantization level precision and the comparator response time variation caused by different input signal levels.

Since a relatively large number of comparators are required, circuit size and power dissipation are usually large. Furthermore, since it is rather difficult to guarantee the same environments for all comparators, attainable resolution is limited to about 8 bits. In order to break this limit, further efforts are required to guarantee the same condition for all comparators and to decrease delay time variation of the incoming signals and clocks.

5.3 High Accuracy Conversion

A successive approximation method and a charge integration method have been mainly used to achieve highly accurate ADCs. Their accuracy is determined by capacitor array precision, and operating speed, respectively.

Recently, oversampling ADC methods have been reported. These approaches have been promoted by development of digital signal processing VLSI and an

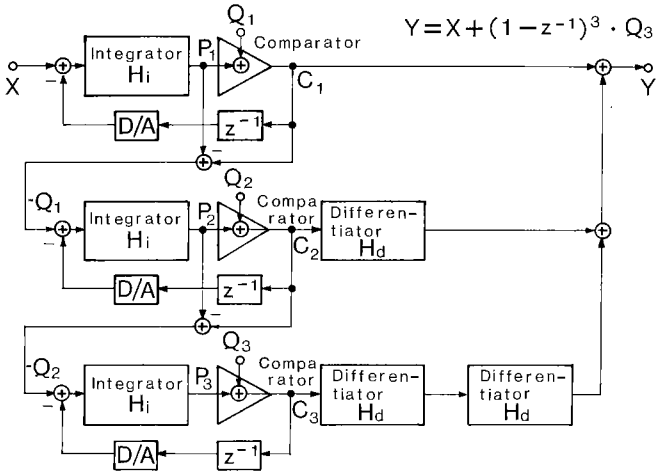

Fig. 13 Three-stage MASH signal flowchart.

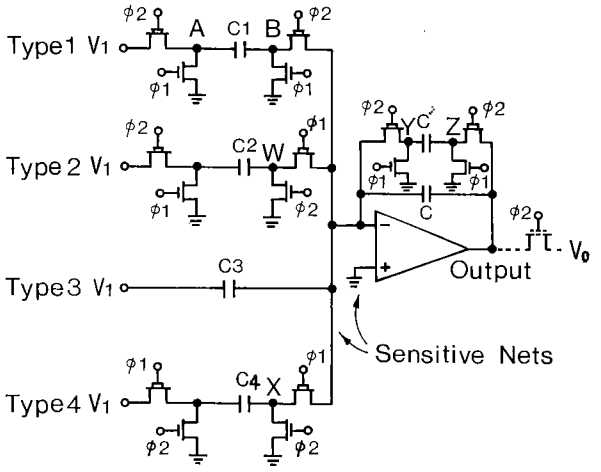

Fig. 14 General first-order strays-insensitive SC building block.

accuracy compensation method in a digital domain[30]. Noise shaping and linear prediction are basic algorithms. They are appropriately combined, resulting in many alternatives.

A multi-stage noise shaping (MASH) ADC is one of the most hopeful method to achieve highly accurate ADCs[31]. This approach can overcome unstable behavior caused in conventional high-order noise shaping ADCs. MASH combines plural 1st-order noise shaping quantizers in a cascade form. A three-stage MASH signal flowchart is shown in Fig. 13. Quantization error in the 1st-stage is transferred to the 2nd-stage. The 2nd-stage output is subtracted from the 1st-stage output in order to cancel the quantization noise This operation is further repeated between the 2nd-stage and the 3rd-stage. Therefore, quantization errors are not extensively amplified, and stable operation is guaranteed for a high-order noise shaping ADC. A 16 bits MASH ADC LSI has been fabricated using a 2 μm CMOS process. A 256 tap FIR digital filter is also integrated on the same chip for sampling frequency reduction. High SNR, more than 91 dB, was obtained without any adjustment. This result demonstrates MASH ADC can be applied to digital audio systems.

6. SC Silicon Compilers

In order to spread integrated analog circuit applications, simplifying LSI design and fabrication process is very important. For this purpose, automatic circuit design and layout techniques have been tried[32]-[34].

6.1 Optimum Design of SC Circuits

Desired filter responses are compiled into a circuit configuration, capacitor values, and requirements for switches, capacitors, and Op-Amps, which will be designed using MOS device. Basic design techniques for individual requirement have been well accomplished. Furthermore, they should be effectively combined to achieve a globally optimum solution. A systematic design rule for this purpose still remains as the research objective.

6.2 MOS Circuit Design

Components used in SC circuits are designed using MOS device, taking the previously obtained specifications into account. Furthermore, requirements for a chip area, power dissipation, the output noise, DC offset voltage, and PSRR are also considered. Design parameters in this step include unit capacitor size, a W/L ratio of an FET switch, Op-Amp performance and its transistor size, resistor type, necessity of dummy components, selection between single-ended or differential circuits, and so on. Requirements for MOS circuit design often conflict with each other. Therefore, best trade-off must be found. A general design rule for this purpose seems to remain as an open question.

6.3 Automatic Layout

Layout is also one of complicated processes, which requires sophisticated know-how to achieve highly accurate performance and good noise immunity. Therefore, it is desirable to carry out this process automatically.

One example for automatic layout is described here[33]. Since SC circuits are usually constructed using a general 1st-order SC building block illustrated in Fig. 14. Each block contains a fixed Op-Amp and switches, and parameterized capacitors sub-blocks. Each Op-Amp is selected from a library, taking capacitive load into account. All capacitors are constructed from unit capacitors and a special variable unit capacitor, and maintain a constant area to perimeter ratio.

Careful layout and design techniques are used to construct these building blocks such that highly connected components are clustered and sensitive net rout-

ing is isolated. This provides the sensitive net isolation, parasitic insensitivity, and noise immunity necessary for good performance. Only large-swing low-impedance amplifier outputs remain to be routed after the block construction has been completed. Furthermore, ground and power supply wires for analog and digital portions are completely isolated. Signal wires are also isolated from ground and power supply wires. Clock signals are usually routed close to small swing analog signals. Their cross wiring should be avoided.

Placement and routing of the blocks are performed by the automatic standard cell layout program. Layout of 7th-order SC lowpass filter was automatically generated. A chip area is only 2% larger than that obtained by manual layout.

7. LSI Customization Methods

Minimizing LSI fabrication cost and term is also important to spread integrated custom analog circuit applications.

7.1 Analog Master Slice

To improve design productivity, the master slice approach for mixed analog/digital circuits has been reported[35]. The LSI consists of gate-isolated type transistor cell arrangements, double poly-silicon passive element structures, channels for high-impedance wires and digital wires. Figure 15 shows basic elements and block layout. Parallel connection of diffusion areas, as in Fig. 15(b), yields a wide-channel transistor, and serial connection, as in Fig. 15(c), produces a long-channel transistor, both useful in analog circuits. Figs. 15(d) and (e) show that double-layered poly-silicon patterns constitute passive elements. Use of two layers offers a capacitor, and the first layer only acts as a resistor. Fig. 15(f) shows a part of a chip layout, on which transistors and passive elements are placed symmetrically with regard to a horizontal line. Chip characteristics are listed in Table 2. A voice-band MODEM LSI for mobile telephone equipment has been developed using this master slice. It includes high-order SC filters, a voltage reference, and a data detector. Passband ripple is less than 0.1 dB. A 60 dB dynamic range is achieved.

7.2 Standard Cell Approach

Another simplified LSI fabrication method is to use standard cells. Functional blocks used in analog circuits, such as Op-Amps, comparators and so on, are designed and stored as standard cells in a library. These analog standard cells are combined with logic cells, resulting in a mixed analog/digital LSI. In this approach, developments of universal standard cells and automatic placement and routing program, by which desired accuracy

Table 2 Chip characteristics.

Technology		Si-gate N-well COMS
Number of transistors		17,000
Number of passive elements		7,300
Number of I/O buffers		128
Total analog filter order(max.)		140
Number of gates(max.)		2,800
Chip size		7.1mm X 7.48mm
Cell transistor size(W/L)	PMOS	27μm/2.8μm
	NMOS	27μm/2.6μm
Unit capacitance		0.5pF
Unit resistance		200 ohms
Power supply		+5V

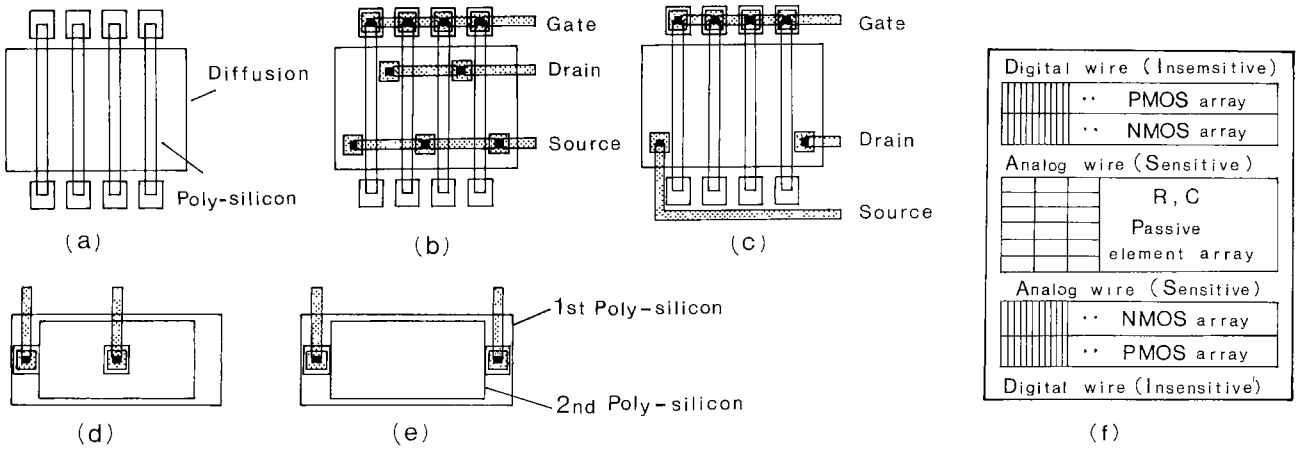

Fig. 15 Mixed analog/digital master slice LSI. Basic cells: (a) gate-isolated-type cell, (b) wide channel transister, (c) long channel transistor. Passive elements: (d) unit capacitor, (e) unit resistor. (f) Cell placement.

and SNR in analog circuits can be obtained, will be further required.

7.3 Programmable Analog Circuits

The simplest LSI fabrication is to use programmable analog circuits. Characteristics for SC circuits can be controlled by a sampling frequency and capacitor arrays. However, obtainable functions are rather limited, compared with digital signal processor implementation. Therefore, this approach will be used to some specific application, such as filters, equalizers, oscillators, and so on.

8. Present and Future Applications[36]

Features of analog circuits, compared with digital circuits, are high speed operation, low power dissipation and high integration density. On the other hand, complicated functions, accurate operation, and programmability are easily provided by a digital approach. They will be appropriately combined in many LSIs, rather than being applied to different systems.

8.1 Analog-to-Digital Interface

Analog-to-digital conversion is a very important technique, even though digital LSI technology makes a great progress. This is because signal sources, transmitted signals over lines, and perceptible signals by human are inherently analog signals. The interface circuits are constructed by combining analog and digital circuits. Analog circuits can be effectively used to construct A/D and D/A converters, pre-filter, post-filter, line equalizer, and so on. Furthermore, signal processor VLSIs with analog I/O functions will be developed extensively.

8.2 High-Frequency Application

A high frequency band, up to several MHz, could be covered by SC circuit technique. 320 kbps digital transmission, facsimile and television systems are included in SC circuit applications. In these systems, many function blocks, i. e., line equalizer, band-limiting filter, vestigial sideband filter, amplitude and delay equalizers, enhancers and comb filter, seem to be candidates for SC circuit realization.

On the other hand, the experimental results demonstrate that video band and VHF band signal processing could be implemented by using bipolar active RC circuits.

Furthermore, higher frequency bands over 100 MHz and 10 GHz could be covered by the wide-band amplifier and MMIC, as mentioned in Sect. 2, respectively. They are designed based on lumped and distributed element models, respectively.

8.3 Low Power Dissipation

Portable communication systems for personal use will be increasingly important. They include, for instance, personal and mobile transceivers, portable telephone systems, pocket-size television sets, etc. Remotely reading several types of meters, e. g., electric, gas, and water meters, through telecommunication systems will also be important. These systems should be miniaturized as much as possible, and should have very low power dissipation.

An internal human conditioning system is fully implantable and can perform all essential functions of measurement and stimulation in human body. In order to guarantee long battery lifetime, power dissipation should be very low. Furthermore, good noise immunity, low distortion, and small size are strictly required. For this purpose, a mixed analog/digital approach using CMOS device is very useful. By relaxing requirements for Op-Amp performance, 190 μW power dissipation for 4th-order SC pre-filter, with 5 kHz cutoff frequency, has been achieved[20].

In low frequency applications, however, digital circuits can also sufficiently decrease power dissipation. So, an analog approach is not always a best choice in this case.

8.4 Other Applications

Recently, new concept for computing and networks has appeared. A neural network consists of a huge number of processing elements, i. e., neurons. Each processing element has many input signals, but only a single output signal. A relation between the output signal and a sum of input signals is nonlinear. The output signal is linearly weighted, and is transferred to many processing elements. If the signals are analog voltages, then the weights can be represented by resistors, and by Ohm's law the intermediate answers are currents; by Kirchoff's law, all these currents can be summed by connecting the currents together at one terminal to give the output. Nonlinearity, such as saturation behavior, is easily realized by using active elements. Since analog elements directly correspond to each neural net element, an analog approach can provide a large scale neural chip, compared with a digital version[37].

A composite system, combining an analog sensor and signal processing, seems a new application of analog circuits. This system could be realized by using three dimensional LSIs.

9. Conclusion

This tutorial paper has provided an overview for the present and future trends in design and applications of integrated analog signal processing circuits. Their

design and fabrication techniques have made a great progress during the recent decade. Since there exist many analog environments, mixed analog/digital LSIs will play an important role. In these system, analog and digital circuits supplement each other's excellent features and negate drawbacks. The design and fabrication techniques, presented in this paper, have not been well accomplished. They include new circuit configuration with reduced sensitivity to nonideal element effects, silicon compilers, globally optimum design rule, and simplified LSI customizing process. The future of integrated analog circuits seems to be highly dependent on their successful accomplishment.

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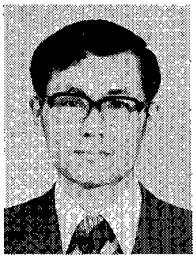

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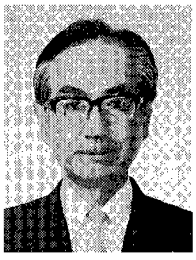

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